AMENDMENT AND RESPONSE

Serial No. 10/017,892

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Title: METHOD AND ARCHITECTURE TO CALIBRATE READ OPERATIONS IN SYNCHRONOUS FLASH

MEMORY

IN THE CLAIMS

Please amend the claims as follows:

(Currently Amended) A flash memory device comprising:

a memory array having erasable blocks of memory cells, each block of memory cells being arranged in a row and column configuration, wherein each column of memory cells is couplable to an associated bit line;

control circuitry to control memory operations to the memory array;

a verify sense amplifier to verify a program state of the memory cells, the verify sense amplifier is coupled to a first location of the associated bit lines;

a read sense amplifier to read a program state of the memory cells, the read sense amplifier is coupled to a second location of the associated bit lines; and a switch to selectively couple either the verify sense amplifier or the read sense amplifier to an output circuit.

- 2. (Original) The flash memory device of claim 1 wherein the flash memory is a synchronous flash memory.
- 3. (Original) The flash memory device of claim 1 wherein the verify sense amplifier and the read sense amplifier have adjustable sensitivity.
- 4. (Currently Amended) The flash memory device of claim 1 wherein the <u>verify read</u>-sense amplifier comprises transistors with a gate oxide of approximately 200 Å and the read sense amplifier comprises transistors with a gate oxide of approximately 70 Å.

Claims 5-14 (Previously Cancelled)

14. (Original) A method of calibrating a non-volatile memory comprising: reading a data state of a plurality of memory cells with a first sense amplifier;

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reading the data state of the plurality of memory cells with a second sense amplifier; comparing outputs of the first and second sense amplifiers to determine offsets between the first and second sense amplifiers; and adjusting either the first or second sense amplifier to calibrate the first and second sense amplifiers.

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- 15. (Currently Amended) The method of claim 14 wherein the 5-wherein the first sense amplifier is used during erase and program operations.
- 16. (Original) The method of claim 14 wherein the second sense amplifier is used during read operations.
- 17. (Original) The method of claim 14 wherein the non-volatile memory is a flash memory.
- 18. (Original) The method of claim 14 wherein comparing the outputs of the first and second sense amplifiers is performed by an external test circuit.
- 19. (Original) The method of claim 14 wherein adjusting either the first or second sense amplifier comprises changing a voltage sensitivity of the sense amplifier.
- 20. (Cancelled)